HX5000 ASIC Platform
S150 (150 nm) ASICs

Honeywell

Advanced Information

GENERAL DESCRIPTION

The Honeywell HX5000 Platform ASICs are manufactured on the Honeywell 150nm CMOS Silicon on Insulator technology using a cell-based library and advanced ASIC design methodology. The design and manufacturing flow supports ASIC development from RTL through delivery of tested ASICs. This very high density ASIC technology supports full range of radiation hardness requirements.

Honeywell's S150 150 nm Silicon on Insulator (SOI) process enables very high density ASICs with gate counts exceeding 8 million usable gates. This is achieved using a fully planarized 6-layer metal process. HX5000 is designed for use over the full military temperature range while operating in harsh radiation environments. The S150 technology is designed to withstand extremely high levels of Total Dose Hardness and the HX5000 ASIC library Flip-flops and SRAM cells are designed for extremely low static and dynamic Soft Error Rate (SER)

The ASIC development methodology that supports these complex ASICs is based on the Synopsys Galaxy™ toolset. This robust design flow supports flexible design handoffs with multiple entry points including specification, RTL, or synthesized gate level netlist. Design For Test (DFT) is an integral part of this design flow.

Each HX5000 design is based on the proven ASIC Library of standard logic elements, module compiler cells, configurable RAMs, and selectable I/O cells. Macro cells such as Phase Lock Loop (PLL) and Delay Lock Loop (DLL) are available as well as access to macros included in Synopsys' DesignWare ® IP.

Designers can choose from a wide variety of I/O types. High speed and standard bus interfaces such as PCI, LVDS, SSTL2 and LVPECL buffers are available. A high speed SerDes is being developed which provides 4.25 Gb/s per channel performance. Standard CMOS I/O cells include buffers with multiple drive strengths, three-state capability, and pull-up/pull-down resistors. The HX5000 product family supports 1.8V, 2.5V, and 3.3V I/O.

Several package types are available including CQFP, LGA, DBGA and FC-LGA.

This family is available with Honeywell's high reliability screening procedures and consistent with Class S requirements. QML qualification is anticipated.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS Technology
- 150 nm Process (Leff = 110 nm)
- Total Dose Hardness: 1x10^{6} rad (Si) available
- Dose Rate Upset Hardness $\gtrsim$ 1x10^{11} rad(Si)/s
- Dose Rate Survivability $\geq$1x10^{12} rad(Si)/s
- No Latch-up
- Ultra Low Power
  - 13 nW/Gate/MHz (1.8V)
- Many I/O Options:
  - 1.8V/2.5V/3.3V CMOS
  - Cold spare
  - PCI
  - 2.5V, 3.3V LVDS
  - 1.0625 to 4.25 Gb/s SerDes
  - SSTL2 Class I and II
- Wide selection of Single- or Dual-Port Drop-In SRAMs
  - Custom SRAM design capability
- 25 MHz to 1.0 GHz Phase Locked Loop (PLL)
- VDSM ASIC Design Methodology based on Synopsys tool set
- Package Signal I/O count:
  - Up to 508 for wire bond
  - Up to 1000 for flip chip
- Operating Voltages
  - 1.8 V $\pm$ 0.15V Core
  - 1.8V, 2.5V and 3.3V I/O
- Operating Range is -55°C to +125°C case temperature

TECHNICAL DESCRIPTION

S150 SOI Description

The Honeywell technical approach for development of HX5000 ASICs utilizes our state-of-the-art 150-nanometer silicon-on-insulator CMOS (S150) technology. SOI CMOS offers advantages for high-performance applications not attainable in standard bulk CMOS for radiation hardened applications. SOI devices are fabricated in a thin film of silicon on top of a buried oxide insulator on top of a standard silicon wafer. SOI has a proven history of resistance to SEU and immunity to latch-up. These advantages simplify fabrication steps, improve density and reduce a variety of parasitic capacitances. SOI also supports lower threshold voltages, compared to bulk CMOS, which equate to higher performance.

Reduced Power Consumption

- SOI technology offers lower capacitance than bulk CMOS of the same feature size results in lower power reduction.
- 1.8V operating voltage of the core and I/O cells.
- High speed serial output cells and macros such as SerDes reduce number of output drivers.

TECHNICAL PARAMETERS

HX5000 Characteristics	Value
Maximum Routable Gates (1)	8 – 12 Million
Maximum I/O Count Wire Bond Die (108 µm pad pitch) Wire Bond Die (75 µm pad pitch) Flip Chip Die (double row)	 388 508 1000
Layers of Metal	6
Minimum Geometry	0.15 µm drawn /0.11 µm L_{eff}
Operating Voltage (Core)	1.8 ± 0.15V
Operating Voltage (I/O)	1.8 ± 0.15V, 2.5 ± 0.2V, 3.3 ± 0.3V
Typical Intrinsic Delay-2 Input NAND (fan out =2)	60 ps @ 1.8V
Typical Power Dissipation, µW/Gate/MHz 20% Data, 200% Clock Activity Rate	0.013 @ 1.8V
Operating Temperature	-55°C to 125°C
ESD (Human Body Model)	>2000 Volts

(1) The S150 technology will be qualified to support a gate count of 8M gates in 2006 and will increase toward 12M gates. The number of routable gates is dependent on several other factors including routing densities, amount of embedded RAM, package type and I/O quantity.

Radiation-Hardness Ratings

Parameter	Limits	Units	Test Conditions
Total Dose	$> 1 \times 10^6$	Rad(Si)	VDD= 1.95 Volts, VDD2= 3.6 Volts T_C = 25C, X-Ray or Co60
Static Soft Error Rate (1) Flip Flop SRAM (Single Port) SRAM (Dual Port)	 $\leq 1 \times 10^{-15}$ $\leq 1 \times 10^{-11}$ $\leq 1 \times 10^{-12}$	 Upsets/bit-day (2) Upsets/bit-day (2) Upsets/bit-day (2)	VDD= 1.65 – 1.95 Volts, VDD2= 3.3 Volts, T_C = 25°C (static clock)
Dynamic Soft Error Rate (1) Flip Flops	 $\leq 1 \times 10^{-9}$	 Upsets/bit-day (2)	VDD= 1.65 – 1.95 Volts, VDD2= 3.3 Volts, T_C = 25°C, Clock Freq = 100 MHz
Transient Dose Rate Upset	$> 1 \times 10^{11}$	Rad(Si)/s	VDD= 1.65 Volts, VDD2= 3.0 Volts T_C = 25°C Pulse Width = 20ns, X-Ray
Transient Dose Rate Survivability	$> 1 \times 10^{12}$	Rad(Si)/s	VDD= 1.95 Volts, VDD2= 3.6 Volts T_C = 25°C Pulse Width = 30 nsec, X-Ray
Neutron Fluence	1×10^{14}	N/cm^2	1MeV equivalent energy

(1) There are multiple types of registers with different SER ratings.
(2) Adams 90% W.C. environment GEO orbit, 100 mil shielding

RADIATION CHARACTERISTIC

Total Ionizing Dose (TID) Radiation

The S150 SOI process technology provides protection against TID effects. Through a combination of the oxide insulation layer, trench isolation and control of the transistor threshold voltages, the SOI reduces charge accumulation and leakage currents in the circuit elements. The HX5000 library will meet all stated functional and electrical specifications when tested in accordance with MIL-STD-883 Test Method 1019. Total dose hardness is assured by wafer level testing of process monitor transistors using a 10 KeV X-ray radiation source. Transistor gate threshold shift correlations have been made between 10 KeV X-rays applied at a dose rate of $1x10^5$ rad(SiO_2)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Dose Rate Transient Radiation

Dose Rate Transient radiation induces high current transients which can lead to circuit upset. The S150 process minimizes the impact of Dose Rate transients through reducing charge accumulation. Additional measures including specialized power bussing and current control techniques are used to minimize the effects of the radiation.

Neutron Radiation

The library elements will meet any functional or timing specification after exposure to the specified neutron fluence under recommended operating or storage conditions.

Single Event Upset

Single event upset radiation events induce localized charge in the circuits. These can cause a change of state in elements like flip flops, latches and embedded RAMs. The SOI process again limits the amount of charge accumulation. The HX5000 library contains several types of storage elements, including registers and embedded RAM, which are designed to be immune to different levels of single event radiation.

Latchup

The HX5000 Library elements will not latch up under any conditions including the above radiation exposure conditions when applied under recommended operating conditions. Fabrication with the SOI substrate material provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR-type latchup structures.

HX5000 LIBRARY

HX5000 library contains over 630 standard cells with a broad array of cell types. Many logic functions have multiple versions available to allow for trade-offs of radiation tolerance, speed, power consumption, and I/O drive strengths. Flip flops and memory cells are available in several SEU levels to support different radiation requirements.

The library also contains a wide range of single and dual port embedded SRAMs and mixed signal macros such as the PLL and DLL. The library is designed to support use of Synopsys Module Compiler™. Module Compiler is a tool for creating high-performance, datapath-intensive modules.

Embedded SRAMs

Honeywell provides a wide selection of SRAMs to embed into your design. This library of predefined macro cells includes both single port and dual port SRAMs. The sizes range from 256 x 8 up to 16,384 x 40. Typical access times are 3 ns.

Honeywell also provides a service to create custom RAMs for unique applications.

I/O Options

Description	Operating Voltages	Max Operating Frequency	Features
CMOS	1.8V, 2.5V, 3.3V	200 MHz (1)	Cold Spare option
PCI	3.3V	33MHz / 66MHz	
LVDS	2.5V, 3.3V	600 Mb/s (1)	Cold Sparing
SerDes (2)	1.8V	4.25 Gb/s per lane 10Gb/s XAUI Mode	8 channel macro cell
SSTL (2)	2.5V	Up to 250 MHz	Class I & II, Input, Output and Bi-pad
LVPECL (2)	1.8V	Up to 1.2GHz (Clock) Up to 1.2Gb/s (Data)	Input only, AC Coupled

Notes:

(1) CMOS I/O operating speeds limited by external board design and loading.

(2) These are in development. Contact Honeywell for availability.

SerDes

To support high speed data communication needs, an 8 channel SerDes (Serializer/Deserializer) macro is being developed. The SerDes implements two main functions: the actual serialize/deserialize of the data and the protocol data formatting and encoding/decoding.

The SerDes I/O macro-cell can transmit and receive date at rates of 1 - 4.25 Gb/s per channel. It includes features to maximize the performance of the data transmission. To improve signal integrity and improve Bit Error Rate (BER), the transmitter has 8-level programmable output drivers and the receiver has 8-level equalization. This allows for reliable communications over 40 inches of backplane or 15 meters of cable. An integrated PLL provides the necessary accuracy and programmability of the internal clocks.

SerDes is designed to support the following standard protocols. The SerDes can be programmed for the correct protocol, format the data, and encode data.

- 10 Gbps Ethernet XAUI and 10 Gbps Fibre Channel XAUI transceivers and MAC layer devices
- 10 Gbps optical transceivers (10Gbase-LX4) and Infiniband cable based copper transceivers (10Gbase-CX4)
- 1.0625 Gbps, 2.125 Gbps and 4.25 Gbps Fibre Channel transceivers, Host Bus Adapters (HBAs), and Switches
- 1.25 and 3.125GBPS Gigabit Ethernet

PLL and DLL

The HX5000 library includes both PLL and fully digital DLL macro cells. The PLL macro cell operates up to 1.0 GHz and the DLL operates up to 1.2 GHz. The DLL cells have four clock outputs each shifted by 90°.

ASIC METHODOLOGY AND CAD TOOLS

The design flow infrastructure for HX5000 ASICs has been developed by Honeywell and Synopsys. This design environment includes:

- Leading-edge Synopsys EDA tools for designing and verifying complex ASICs
- A flexible set of front-end and back-end design services from design teams expert in the implementation of advanced ASICs and the HX5000 design flow
- A secure, web-based design environment with scalable compute resources that enables collaboration from multiple sites
- Access to intellectual property (IP) cores from Honeywell and Synopsys' DesignWare® IP, to accelerate design time and reduce development costs.
- Qualified standard-cell libraries supporting both rad-hard and rad-tolerant designs

The collaborative design environment created by Honeywell and Synopsys provides a development model that is far more flexible than traditional ASIC options. Along with support for traditional and expanded ASIC handoff options, implementation support may include design services available from Honeywell and Synopsys Professional Services in a fully collaborative design model.

DESIGN COLLABORATION ENVIRONMENT (DCE)

With the level of device densities that are possible with 150-nm rad hard ASICs, the infrastructure must effectively manage data, hardware and software resources. Design teams and resources with highly specialized skills are distributed amongst multiple sites and during critical stages of the design, peak compute requirements often introduce bottlenecks.

To support this level of ASIC development, Honeywell and Synopsys have established the Design Collaboration Environment (DCE). The DCE enables multiple users to access a common design database. In addition to real-time and secure sharing of design data, the DCE also provides on-demand access to all the design tools, along with extensive compute and storage capacity. The DCE enables engineers at multiple remote locations to act together as a single design team with a unified design database and flow, applying the best expertise regardless of geography or time zone.

The tools supported under the DCE are based on Synopsys Galaxy and Discovery platforms. The flow also includes procedures and tools to assess radiation performance, signal integrity, cell EM (electromigration) analysis, and rad-hard power plan methods.

ASIC Development Flow

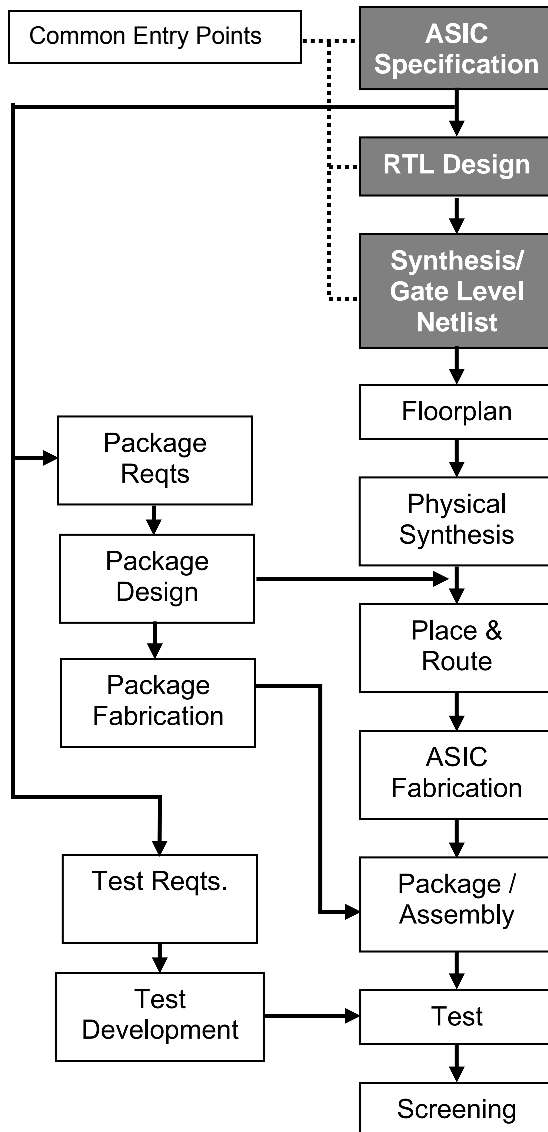
The ASIC development flow processes a design from the ASIC specification through tested ASIC delivery. For ASIC designs that push the performance envelop, the flow is configured to support preliminary synthesis and place and route, termed "advanced prove-out", to converge on an optimized design which meets all the performance constraints. The requirements associated with packaging and test are also addressed as part of the ASIC development.

Design For Test (DFT)

Honeywell has integrated Design For Test (DFT) into the HX5000 ASIC Development Flow. It encompasses Memory Built In Self Test (MBIST), Scan/Boundary Scan, ATPG, and Functional test. It is designed to be a complete test process that allows for simulation and hardware test to use the same functional test vectors. The DFT flow is supported by tools from Logic Vision, Synopsys and Credence.

ASIC Development Flow Diagram

Typical entry points include RTL, Gate Level Netlist, and Specification.



DFT

Memory BIST Insertion into RTL
Memory BIST collars around the embedded RAMs in the RTL design. Inserts a top level control system utilizing an 1149.1 JTAG TAP, insert IO boundary-scan, and run MBIST tool verification steps.

Synthesis
The scan control structures are inserted. Provide an initial scan-chain ordering to support the "Scan Evaluation" step.
Perform initial ATPG (Automatic Test Pattern Generation) scan vector generation.

Physical Synthesis
Create logical order of the scan chains on the physical placement of the cells.

Post Route Test Vector Generation

Scan Vector Creation & Simulation
Generate the full ATPG test vector set and verification test bench.

Memory BIST Vector Creation & Simulation
Simulations to validate the correct functionality of the TAP controller, boundary-scan, access to and basic functionality of the MBIST controllers.

DC Vector Creation/Simulation
Create vectors to perform parametric testing of an ASIC.

Functional Vector Creation/Simulation
Create vectors that verify the functional performance of the ASIC.

Vector Verification
Perform basic verification that the vector files produced to test an ASIC meet tester compatibility requirements.

Vector Translation
Convert industry standard formats (WGL & VCD) into a format that is compatible with Honeywell testers.

PACKAGING

Honeywell can provide a wide variety of single chip packages for HX5000 ASICs. The primary form factors are ceramic quad flatpacks (CQFPs) up to 352 pins, and area array packages (land grid arrays or dimpled ball grid arrays), currently up to 783 pads. Most of our packages conform to JEDEC standard outlines.

Honeywell can personalize standard package outlines to accommodate a variety of die footprints, pin assignments, or routing requirements. Honeywell can also design custom single chip or multi-chip modules.

Honeywell's package designs meet a wide range of thermal, electrical, and mechanical performance requirements. Thermal resistances (junction-to-board) of approximately 1 °C/Watt are typically achieved for 15mm die sizes in LGAs or CQFPs. Honeywell can provide thermal or electrical modeling of package characteristics as part of the package design.

Package Construction and Assembly Processes

All of our standard ceramic packages are hermetically sealed, screened and qualified to MIL-PRF-38535 Class S or V requirements. The table below summarizes the basic materials and assembly methods for Honeywell's qualified, wire bonded ceramic packages.

HERMETIC CERAMIC PACKAGE PARAMETERS

Feature	Description	Feature	Description
Package Body	90% Alumina (Al203)	Leads, Seal Ring	Kovar (Fe-Ni-Co) with CuAg braze
Internal Metallization	Tungsten or Molybdenum	Lid	Kovar or Ceramic
Metal Layers	Up to 17 layers for signal routing and Power\ Ground distribution	Die Attach	Cyanate ester
External Metallization	Nickel-gold plating	Wirebond	Ultrasonic Al Wedge Bond
		Hermetic Seal	AuSn solder seal

FLIP CHIP PACKAGING

For ASICs with very high I/O count (>508 I/O), flip chip packages are available. In flip chip packaging, the chip-to-package connections are made through an array of solder bumps patterned over the area of the die, rather than wire bonds around the perimeter of the die. This technology extends the available I/O count to 1000 per die, and also improves the electrical, thermal, and radiation performance of the package ASIC. Our flip chip technology is based on high reliability materials and design rules. It uses a polyimide repassivation layer on the die, high-temperature, low alpha emitting 95/5 Pb/Sn solder bumps, and an organic underfill between the die and package. Packages for flip chip devices are typically ceramic land grid arrays, and do not require a hermetic lid seal. Our flip chip packages meet Moisture Sensitivity Level 1, and will be qualified to Mil-PRF-38535, Appendix H guidelines.

TEST CAPABILITIES

Honeywell HX5000 test capabilities include wafer and packaged part level testing. Testing capabilities encompasses the complete Class S screening flow. The test platform is based on testers manufactured by Credence among others and includes the EXA3000-800 digital tester.

The EXA3000-800 has a maximum of 1024 digital I/O pins. These consist of 960 channels that are single-ended and have a maximum data rate of 800Mbps. It also has 32 differential channels supporting rates up to 3.2Gbps data rates.

This tester has pin and system level Precision Measurement Units (PMU), timing measurement unit, Sequencer Per Pin (SPP) pattern generator used for digital functional testing, and a 3.2Gbps Wavecrest SIA.

The EXA3000 test system is also designed to support true mixed-signal test techniques using a patented analog channel architecture that is integrated with the digital sub-system. It is equipped with two BroadBand Channel (BBC) instruments and a High Accuracy (HA) instrument.

RELIABILITY

For more than 15 years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered thousands of QML parts since first becoming QML qualified in 1990.

Using this proven approach Honeywell will assure the reliability of the S150 products. This approach includes adhering to Honeywell's General Manufacturing Standards for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, negative bias temperature instability, radiation)
- Utilizing a structured and controlled design process
- A statistically controlled wafer fabrication process with a continuous defect reduction process
- Individual wafer lot acceptance through process monitor testing (includes radiation testing)
- The use of characterized and qualified packages
- A thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

QUALIFICATION AND SCREENING

The S150 technology is qualified by Honeywell after meeting the criteria of the General Manufacturing Standards. This approval is the culmination of years of development and requires a considerable amount of testing, documentation, and review. It is planned to QML certify the S150 technology and HX5000 products. This requires additional testing, documentation, and DSCC approval.

The test flow includes screening units with the defined flow (Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups B, C, D, and E). Both the S150 process and individual product are subject to period or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests, respectively.

Group A	General Electrical Tests
Group B	Mechanical - Dimensions, bond strength, solvents, die shear, solderability, Lead Integrity, seal, acceleration
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package related mechanical tests - Shock, Vibration, Accel, salt, seal, lead finish adhesion, lid torque
Group E	Radiation Tests

Honeywell delivers products that are tested to meet your requirements. Products can be screened to several levels including Proof of Design (POD), Engineering Models, and Flight Units. PODs and EMs are available with limited screening for prototype development and evaluation testing.

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