High Temperature SOI CMOS Electronics Development

The Deep Trek Project

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1. Introduction

The absence of high temperature electronics is an obstacle to the development of untapped energy resources (deep oil, gas, and geothermal). This paper describes a project under the U.S. Dept. of Energy's Deep Trek program to develop SOI CMOS processes and design platforms targeted to meet this need. Deep Trek is a technology development program to enable drilling systems for the extreme conditions that are encountered in tapping deep natural gas reservoirs. The program is administered by the Strategic Center for Natural Gas (SCNG), which is an organization of the National Energy Technology Laboratory. The objective is to dramatically reduce the cost and risk of drilling to depths of 20,000 feet or more. To put this in perspective, more than 70% of current natural gas production is from wells that are less than 5,000 feet deep. The Deep Trek program has funded multiple projects and multiple technologies since 1997. Projects have been funded to address tubing materials, cements, drilling fluids, and electronics tools which show the technical application diversity of the Deep Trek program scope.

This Deep Trek project is awarded to Honeywell International and is managed from Honeywell's Defense and Space Electronic Systems organization. The goal of this project is to commercialize high temperature building blocks chips that are specified by the JIP membership (Oil and Gas Service and Operators, Aerospace & Down Hole Instrumentation Companies) and to provide and high temperature process and tool kit infrastructure to enable future down hole electronics exploration and production electronic needs.

2. Deep Trek Program Need For A High Temperature Electronics Project

U.S. natural gas consumption is projected to grow from 22 trillion cubic feet (tcf) per year in 1999 to 34 tcf in 2020. Cumulatively this is 607 tcf of consumption by 2020, while recoverable reserves using current technology are 177 tcf. A significant portion of this shortfall may be met by tapping deep gas reservoirs. U.S. sedimentary reservoirs more than 15,000 feet deep may contain up to 130 tcf of natural gas according to the SCNG [1,2]. Tapping these reservoirs represents a significant technological challenge. At these depths temperatures and pressures are very high, and may require penetrating very hard rock. Logistics of supporting 20,000 ft. drill strings and the drilling processes are complex and expensive. At these depths up to 50% of the total drilling cost may be in the last 10% of the well depth. Thus, as wells go deeper it is increasingly important that drillers are able to monitor conditions down-hole such as temperature, pressure, heading, etc. It has been estimated that the market for high temperature directional drilling services is a one ($1) to three ($3) billion dollar market [3].

Commercial silicon integrated circuits are rarely specified to operate above 125C and therefore do not meet Deep Trek temperature requirements (175°C to 225°C). A few specialty products are specified for 150C. Down-hole tool providers have been able to "get by" at temperatures up to 175C by screening at temperature electronic parts designed for lower temperatures. Screening components is expensive and using components designed for low temperatures creates system reliability problems [4]. Furthermore, because of economies of scale, the electronic industry trends are against the need for wider operating temperature range. Despite this situation, it has been shown that current technology is capable for high temperature electronics. High temperature effects in bulk CMOS technology have long been studied and design strategies have been developed [5-8] to use bulk CMOS for analog applications in the 200°C to 225°C range [9-11], and in one case even to 300°C [12]. However, these approaches require considerable design skill and expertise and have not resulted in high temperature "Commercial-Off-The-Shelf" (COTS) product offerings. SOI is also frequently cited as a solution for high temperature (>175°C). It is well known that SOI has a number of advantages over conventional bulk CMOS. Both fully depleted (FD) and partially depleted (PD) SOI have been characterized and proposed for high temperature [13-17]. The high temperature advantage derives primarily from the reduction in P-N junction area, and numerous circuit examples have been reported [18-25].

Still, in most cases this has not resulted in commercially available electronic components available to tool developers and down-hole service companies. Why is this? This is not just an oil and gas industry issue: there are other applications for high temperature electronics [26,27], such as distributed controls for avionics, internal combustion engines, geothermal, etc. It seems that high temperature integrated circuits

are not a core business for any of the companies operating in these markets, and that the IC volumes are too low to motivate the IC industry to develop infrastructure to support high-temperature COTS electronics. In other words, the fact that high-temperature electronics have not "taken off" is not a technical failure as much as it is a market failure. The DeepTrek High Temperature Electronics program seeks to overcome this historical "chicken and egg" conundrum by direct investment in high temperature IC technology and infrastructure while simultaneously developing electronic components generally applicable to a wide range of down-hole tools and instruments.

3. High Temperature Electronics Deep Trek Program Goals Objectives and Priorities

The direction and prioritization of implementation for this project is from the JIP project membership. Through their direction, the high temperature electronics chips are specified along with their prioritization of need. The interaction of the JIP membership accomplishes the fundamental market need and fulfilment of that need comes from the JIP membership chip specifications and Honeywell's Defense and Space Electronic Systems organization process development and chip design capability. Furthermore, the JIP membership financially contributes to the project and are hence guaranteed that chip development and samples remain within the JIP membership until commercialization is realized.

Project objectives include: (1) establishing a production-level, high-temperature integrated circuit fabrication process for implementing advanced analog as well as digital functions; (2) making this technology available to the high-temperature electronics JIP membership by providing foundry access as well as by offering Application Specific Integrated Circuit (ASIC) design platforms; (3) developing and putting into production key electronic standard building block functions and chips; (4) ensuring relevance and acceptance of this technology and products by collaboration with industrial partners.

Project Development Priorities:

1. 0.8 Micron High Temperature Mixed Signal Process (HTMSP)
2. Tool Kit for (HTMSP)
3. Programmable Memory
- **A. Development of HT memory process**
- **B. Development of HT memory device (Floating Gate)**
- **C. Development of HT memory product**

4. Re-programmable (volatile) FPGA
5. Precision Amplifier
6. Sigma-delta A-to-D Converter

4. High Temperature Electronics Deep Trek Project's Plan, Risk Management, and Status

1 & 2. <u>0.8 Micron High Temperature Mixed Signal Process (HTMSP) and Tool Kit for (HTMSP)</u>
Plan: Utilize Honeywell's Defense and Space Electronic Systems (DSES) strengths that reside at facility in Plymouth, Minnesota (formerly known as the Honeywell Solid State Electronics Center) is the leading supplier of radiation-hardened SOI digital CMOS integrated circuits. Additionally, capitalize on the previous high temperature electronics developments namely the present commercialization of high temperature electronics and those existing high temperature digital and analog processes to reduce risks

Secondly take full advantage of the synergy between technology developed for high temperature markets and SOI CMOS technology developed for U.S. Government applications, primarily the Department of

Defense. Honeywell's Defense and Space Electronic Systems (DSES) facility in Plymouth, is the leading supplier of radiation-hardened SOI digital CMOS integrated circuits. Both Honeywell and the U.S. Government continue to make investments in SOI technology to meet the strategic needs of the aerospace and defense community.

Honeywell has leveraged the aerospace technology investment by developing derivative processes and product lines, including high temperature electronics. A 1.2 micron IC process with analog features has been used to develop primarily linear products, while a 0.8 micron digital IC process has been used to develop primarily digital products (Table 1). These products feature -55ºC to 225°C performance specifications and are designed for continuous operation for up to 5 years at 225°C [28]. This means that all products are 100% tested to specifications at 225°C prior to shipment (after burn-in, usually at 250°C).

The U.S. government and Honeywell have since made additional investments to develop mixed-signal ASIC capability using 0.8 micron SOI technology (i.e., analog features and library cells have been added to a digital IC process flow). This presents the opportunity for extending this capability from radiation-hardened aerospace applications to commercial high temperature applications. The main steps to accomplishing this are :

(1) Remove process steps included strictly to render the process radiation hard (a requirement to avoid U.S. export restrictions),
(2) Re-targeting the threshold voltage implants to address sub-threshold leakage and render the technology functionally useful for up to 300°C;
(3) Modelling and library characterization for extension to high temperature.
(4) Remove process steps included strictly to render the process radiation hard (a requirement to avoid U.S. export restrictions),
(5) Re-targeting the threshold voltage implants to address sub-threshold leakage and render the technology functionally useful for up to 300°C;

Table 1, shows comparisons of the existing processes and the new production released 5V SIO4 Process.

Table 1 : SOI Processes / Features Applied to High Temperature

	High Temp 5V SOI4 Digital Process (existing flow)	**Radhard 5V SOI4 Mixed-Signal Process (existing flow)**	**High Temp 5V SOI4 Process Production released**
Gate Oxide	150 angstroms	150 angstroms	150 angstroms
Max. Gate Ox. Voltage	5v	5v	5v
Target Vtn/Vtp	1.2V / -1.3V	0.8 / -0.75V	1.2V / -1.3V
Min transistor length	0.8 microns	0.8 microns	0.8 microns
# of metal layers	3 or 4	3 or 4	3 or 4
Top Si Thickness	0.3 microns	0.3 microns	0.3 microns
Buried Oxide	0.4 microns	0.4 microns	1.0 microns
Partially/Fully depleted	Partially depleted	Partially depleted	Partially depleted
Lithography	5X	5X	5X
DMOS option	No	Yes: >30V VDS	Yes: >30V VDS
CrSiN resistors	No	Yes	Yes
Linear Cap Implant	No	Yes	Yes
Laser trim fuse links	No	Yes	Yes
Lateral PNP VREF	No	Yes	Yes
Total Dose Hardened	No	Yes (1MRad, Si)	No

Status: A high temperature mixed signal processes has been fully developed and tested to prove its capability at -55ºC to 225ºC. Additionally a tool kit and library are available to meet foundry and ASICs needs of the JIP membership.
Tool Kit and Library:
HTSOI4 technology documentation to support custom design
Layout rules, electrical rules, SPICE models

Cadence PDK full-custom development library

Supports Cadence schematic capture, simulation, layout and verification tools

HTSOI4 PDK User's Guide available

Cadence SSI and I/O library

Cadence schematics/layouts for gate-level primitives and rudimentary I/O

HTSOI4 Custom Design Kit and SSI datasheets available

Honeywell VDS Toolkit

Supports HT2000 gate-array based digital IC development

HT2000 Digital Cell Library Databook* available

3. Programmable Memory

Plan: A high temperature Electrically Erasable Programmable Read Only Memory (EEPROM) has only been historically demonstrated in laboratories and a 225ºC production commercialized version has not been available. Therefore this implementation is and still is the highest risk chip being developed under this Deep Trek High Temperature Electronics Project. This significant risk warranted the need for a process and memory consultant to be added to the Honeywell team. Additionally, since the high temperature EEPROM had never been done before it required a step by step implementation so as to not waist funding if on the serial step toward implementation was not realized. A three step development plan was determined. The three serial steps are 3A). Development of HT memory process 3B). Development of HT memory device (Floating Gate) and 3C). Development of HT memory product.

3A. First, a high temperature process would need to be proved that was capable of a device hold a charge for long lengths of time. Additionally, a tunneling thru an oxide had to be implemented to allow a gate to be charged, maintain that charge and be able to be erased. Honeywell would develop or modify its existing process via a test chip layout that had all the required devices proven so the next step B could be taken.

3B. Secondly, a miniature memory device had to be determined that would prove all the high risk circuits required to ultimately achieve a 256,000 Kbit EEPROM. This miniature memory circuitry would be designed and called test chip two. Test chip two would be processed and then high temperature tested to determine its read and write capability. Further more the length of charge retention at high temperatures and ability to be rewritten would have to be proven along with additional circuitry. Test chip two will be designed to show the capability of 1). fabricating a large array of memory cells that can be individually accessed (written, read), 2). high voltage circuits necessary to support row and column interfaces and 3). high voltage oxide will withstand the stressing.

Configuration of test chip two demo memory is: 32 Kbit, Organized into 512 rows by 64 columns, 12 Address Bits, 8 Data I/O Bits and is 1/8th of planned 256 Kbit EEPROM Product.

3C. Lastly, a fully functional 256 Kbit EEPROM product would be designed if steps 3A and 3B were successfully achieved. Honeywell planned for two wafer processing runs. Planning two runs allows for re-design updates and design improvement identified by the previous wafer processing run (3A).

Status: The process (3A) has been proven and charge retention has be demonstrated for 3500 hours at 250ºC. Additionally the test data supports the possibility of over 10,000 hours of charge retention. Testing was stopped after completion of 3500 hours to allow the design team to focus on design of test chip two (miniature floating gate memory). 3A, the first step is a complete success!

The design and layout of a miniature memory device (3B) that addresses all high risk circuitry has been completed. This miniature memory (test chip #2) is now in processing and is expected to complete wafer processing and out for testing in October 2005.

4. Field Programmable Gate Array (FPGA)

Plan: This 30,000 gate FPGA was a high risk item so Honeywell's approach was to use a Honeywell design team that has implemented this ATMEL 6010 design architecture two times previously and in both cases the design was a flawless success. However, due to the different mixed signal 0.8 micron process size and the long and narrow foot print required for down hole exploration measurement tools (wire line or measurement while drilling), modifications of previous layouts had to be made. These layout modifications allowed the design to fit within a prescribed 0.500 inches maximum width while still being

pin for pin compatible with the ATMEL 6010. Operational speed up to 10 MHz clock frequency with a goal of 20 MHz. Maximum configuration clock (CCLK) frequency is 1 MHz.

Status: The design and layout of the FPGA has been completed and this product is now in first pass wafer processing and is expected to complete wafer processing and out for testing in October 2005.

5. Precision Amplifier

Plan: This precision amplifier will have to have a rock solid voltage reference for the precision. Honeywell team feels risk lowered by doing all the design with Honeywell design engineers.

Status: 100% functional first pass success. Product samples distributed to JIP membership in high temperature ceramic packages. Functionality tested in ceramic packages at 250ºC and down hole application tested at 300ºC. Life testing over temperature underway and final report on chip performance over temperature for 2000 hours will be available to JIP membership at next quarterly meeting.

6. Sigma-delta Analog-to-Digital Converter (ADC)

Plan: This high temperature 18 bit sigma delta ADC is high risk as this precision has not been commercialized as a high temperature product. The high temperature adds additional risk coupled with the 18 bit precision requirement. To manage this risk Honeywell added Oak Ridge National Laboratory (ORNL) Consultants to the team. ORNL has demonstrated 18 bit sigma delta functional block at lower temperatures and has equipment to test for that precision.

Status: The design and layout of the 18 bit ADC has been completed and this product is now in first pass wafer processing and is expected to complete wafer processing and out for testing in October 2005.

5. Long Life Attributes of High Temperature Electronics

Products processes on the high temperature electronics process will at lower temperature of operation (<225ºC) have greater reliability and longer life. The high temperature process and it's products, will have a life expectancy of five (5) years of continuous duty at 225ºC. Data, using the most likely failure mode of electro-migration, identifies that at continuous operation at 175ºC would increase life expectancy to approximately ten (10) to fifteen (15) years of life and at 150ºC fifteen (15) to twenty (20) years of life.

This attribute of long life is also portrayed by running a light bulb at lower voltages. When a light bulb is operated at lower voltages, the life expectance is significantly increased. Hence, the use of this high temperature SOI technology at less than 225ºC will have additional life. High temperature electronics should be considered for lower operating temperatures applications such as down-hole production completion management, avionics critical flight systems and where substantial financial loss can be incurred by an electronics failure. In all these applications, long life is a desired attribute and could be achieved by using high temperature electronics designed on a high temperature process. Using high temperature electronics would achieve significant financial payoff in these applications.

6. Project Summary

1) 2007 commercialization is on track for the EEPROM, FPGA, Precision Operation Amplifier and the 18 bit sigma delta analog to digital chip. Additionally, foundry and high temperature library will be available to general public at that time. JIP membership has exclusive access to chips and processes prior to commercialization.
2) High temperature mixed signal process is production released along with tool kits and libraries.
3) Precision Operational Amplifier is 100% first pass success. Functionality operational to specifications up to 250ºC, and successfully field tested at 300ºC. High temperature packaged samples provided to membership. Life testing is underway at Honeywell and is expected to be completed by November, 2005.

4) Processing underway for EEPROM test chip #2 (miniature memory to prove read, write and other high risk functionality), FPGA and 18 bit sigma delta analog to digital converter. All expected to complete processing by October 2005 and then begin testing.
5) Inherent in the use of the high temperature mixed signal SOI processing and resulting designs, is the high reliability coupled with more than five years of life if operated at lower temperatures (<225ºC).

7. Joint Industrial Partners (JIP) project membership

BAKER HUGHES, BP, GOODRICH AVIONICS, HALLIBURTON, HONEYWELL INTERNATIONAL, NOVATEK, QUARTZDYNE AND SCHLUMBERGER.

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